Position (Job title) VLSI Design Engineer	**Reporting HOD**
Department R & D	**Experience 0-1 Year**
Location -Pune	**Qualification – BE/ME Electronics**
	Skill Required 1. BE/ME in Electronics. 2. Experiance in logic design & RTL coding. Verilog HDL /VHDL is must. 3. Experience with synthesis flow. 4. Knowledge of working with different protocols. 5. Experience working with multiple clock domains. 6. Innovative problem solving skill. 7. Strong communication skills and cross functional team work
Core Responsibility	**Responsibility** The position requires strong knowledge of FPGA designing flow. The candidate must have good RTC designing skills and code debugging skills. **1.** Candidate will be responsible for lactic designing and RTC coding for the same to meet requirement**.** **2.** The candidate will be responsible for handling cross /functional team meeting and working with hardware and software designing team. **3.** Ability to work independently and working experience with Xilinx environment is an advantage.